IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application: **Johns et al.**	§	Group Art Unit: **2181**
	§	
	§	
Serial No.: **10/809,553**	§	Examiner: **Lee, Chun Kuan**
	§	
Filed: **March 25, 2004**	§	Attorney Docket No.: **AUS920030696US1**
	§	
For: **Method to Provide Cache**	§	Customer No.: **50170**
Management Commands for a DMA	§	
Controller	§	

PROPOSED AMENDMENT

Please consider the following proposed amendments:

1. (Currently Amended): A system to provide software program control of cache
management, comprising:

a <u>control</u> processor ~~configured to generate DMA commands for the management
of a cache on the execution of a software program on the processor~~; [[and]]

<u>one or more asymmetric processors;</u>

<u>a shared system memory;</u>

<u>one or more local memories, wherein each of the one or more local memories is
associated with a respective one of the one or more asymmetric processors;</u>

a [[DMA]] <u>direct memory access (DMA)</u> controller coupled to the <u>control</u>
processor <u>and the one or more asymmetric processors</u>, configured to execute [[the]]
DMA commands ~~for the management of a cache~~ <u>for moving data between the shared
system memory and the one or more local memories; and</u>

<u>a DMA cache coupled to the DMA controller configured to cache data being
moved between the shared system memory and the one or more local memories;</u>

<u>wherein the control processor is configured to generate DMA cache management
commands for the management of the DMA cache;</u>

wherein the DMA cache management commands comprise at least one of a data cache range touch command that indicates to the DMA controller that the control processor will probably issue a get command for a specified address range, a data cache range touch for store command that indicates to the DMA controller that the control processor will probably issue a put command for a specified address range, a data cache range set to zero command that sets a range of storage specified by an effective address and transfer size to zero, a data cache range store command that indicates a data block specified by an effective address and transfer size to be written to the shared system memory if the data block is considered modified, and a data cache range flush command that indicates a data block specified by an effective address and transfer size to be written to the shared system memory and invalidated in caches of all processors if memory coherency is required and the data block is modified.

2-8. (Canceled)

9. (Currently Amended): A method for cache management in a system comprising a DMA controller and a processor, the method comprising the steps of:

running software on [[the]] a control processor to generate [[DMA]] direct memory access (DMA) commands for ~~management of a cache~~ moving data between a shared system memory and one or more local memories, wherein each of the one or more local memories is associated with a respective one of one or more asymmetric processors;

issuing the DMA commands to the DMA controller; and

executing the DMA commands, wherein the DMA controller is coupled to a DMA cache configured to cache data being moved between the shared system memory and the one or more local memories,

wherein the control processor is configured to generate DMA cache management commands for the management of the DMA cache;

wherein the DMA cache management commands comprise at least one of a data cache range touch command that indicates to the DMA controller that the control processor will probably issue a get command for a specified address range, a data cache range touch for store command that indicates to the DMA controller that the control

processor will probably issue a put command for a specified address range, a data cache range set to zero command that sets a range of storage specified by an effective address and transfer size to zero, a data cache range store command that indicates a data block specified by an effective address and transfer size to be written to the shared system memory if the data block is considered modified, and a data cache range flush command that indicates a data block specified by an effective address and transfer size to be written to the shared system memory and invalidated in caches of all processors if memory coherency is required and the data block is modified.

10-14. (Canceled)

15. (Currently Amended): A computer program product for cache management in a system comprising a DMA controller and a processor, the computer program product having a computer storage medium with a computer program embodied thereon, the computer program comprising:

computer code for running software on [[the]] a control processor to generate DMA commands for management of a cache moving data between a shared system memory and one or more local memories, wherein each of the one or more local memories is associated with a respective one of one or more asymmetric processors;

computer code for issuing the DMA commands to the DMA controller; and

computer code for executing the DMA commands, wherein the DMA controller is coupled to a DMA cache configured to cache data being moved between the shared system memory and the one or more local memories,

wherein the control processor is configured to generate DMA cache management commands for the management of the DMA cache;

wherein the DMA cache management commands comprise at least one of a data cache range touch command that indicates to the DMA controller that the control processor will probably issue a get command for a specified address range, a data cache range touch for store command that indicates to the DMA controller that the control processor will probably issue a put command for a specified address range, a data cache range set to zero command that sets a range of storage specified by an effective address

and transfer size to zero, a data cache range store command that indicates a data block specified by an effective address and transfer size to be written to the shared system memory if the data block is considered modified, and a data cache range flush command that indicates a data block specified by an effective address and transfer size to be written to the shared system memory and invalidated in caches of all processors if memory coherency is required and the data block is modified.

16-21. (Canceled)

22. (New): The system of claim 1, wherein responsive to receiving the data cache range touch command, the DMA controller attempts to bring the range of data identified by an effective address and transfer size of the data cache range touch command into the DMA cache.

23. (New): The system of claim 1, wherein responsive to receiving the data cache range touch for store command, the DMA controller attempts to bring the range of data identified by an effective address and transfer size of the data cache range touch for store command into the DMA cache.

24. (New): The system of claim 1, wherein responsive to receiving the data cache range set to zero command, the DMA controller gets ownership of cache lines associated with an area of the shared system memory and zeroes data in the DMA cache such that the area of shared system memory is effectively zeroed.

25. (New): The system of claim 1, wherein responsive to receiving the data cache range store command, the DMA controller writes the data block to the shared system memory if the data block is modified.

26. (New): The system of claim 1, wherein responsive to receiving the data cache range flush command, the DMA controller writes the data block to the shared memory and

invalidates the data block in caches of all processors if memory coherency is required and the data block is modified.

27. (New): The method of claim 9, wherein responsive to receiving the data cache range touch command, the DMA controller attempts to bring the range of data identified by an effective address and transfer size of the data cache range touch command into the DMA cache.

28. (New): The method of claim 9, wherein responsive to receiving the data cache range touch for store command, the DMA controller attempts to bring the range of data identified by an effective address and transfer size of the data cache range touch for store command into the DMA cache.

29. (New): The method of claim 9, wherein responsive to receiving the data cache range set to zero command, the DMA controller gets ownership of cache lines associated with an area of the shared system memory and zeroes data in the DMA cache such that the area of shared system memory is effectively zeroed.

30. (New): The method of claim 9, wherein responsive to receiving the data cache range store command, the DMA controller writes the data block to the shared system memory if the data block is modified.

31. (New): The method of claim 9, wherein responsive to receiving the data cache range flush command, the DMA controller writes the data block to the shared memory and invalidates the data block in caches of all processors if memory coherency is required and the data block is modified.

32. (New): The computer program product of claim 15, wherein responsive to receiving the data cache range touch command, the DMA controller attempts to bring the range of data identified by an effective address and transfer size of the data cache range touch command into the DMA cache.

33. (New): The computer program product of claim 15, wherein responsive to receiving the data cache range touch for store command, the DMA controller attempts to bring the range of data identified by an effective address and transfer size of the data cache range touch for store command into the DMA cache.

34. (New): The computer program product of claim 15, wherein responsive to receiving the data cache range set to zero command, the DMA controller gets ownership of cache lines associated with an area of the shared system memory and zeroes data in the DMA cache such that the area of shared system memory is effectively zeroed.

35. (New): The computer program product of claim 15, wherein responsive to receiving the data cache range store command, the DMA controller writes the data block to the shared system memory if the data block is modified.

36. (New): The computer program product of claim 15, wherein responsive to receiving the data cache range flush command, the DMA controller writes the data block to the shared memory and invalidates the data block in caches of all processors if memory coherency is required and the data block is modified.

REMARKS

Claims 1, 9, 15, and 22-36 are pending. Claims 1, 9, and 15 are amended. Claims 2-8, 10-14, and 16-21 are canceled. Claims 22-36 are added. Reconsideration of the claims is respectfully requested.

It is respectfully urged that the subject application is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

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